Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **A1**
2. **Y1**
3. **A2**
4. **Y2**
5. **A3**
6. **Y3**
7. **GND**
8. **Y4**
9. **A4**
10. **Y5**
11. **A5**
12. **Y6**
13. **A6**
14. **Vcc**

**.048”**

**9 10 11 12 13**

**7**

**8**

**6 5 4 3 2**

**1**

**14**

**MASK**

**REF**

**HC 04**

**.046”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref: HC 04**

**APPROVED BY: DK DIE SIZE .046” X .048” DATE: 8/24/20**

**MFG: MOTOROLA THICKNESS .014” P/N: 54HC04**

**DG 10.1.2**

#### Rev B, 7/19/02